Name of Project: **ATM Controller**

Designing a Mealy FSM for an ATM Controller as part of CS225/CS226 Project

Implemented in **Verilog** and tested using **ModelSim** for Simulation time of 950ns.

**List of Files attached**:

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| ATM\_Controller\_Video.mp4 | Video for explaining the project |
| ATM\_Controller.pptx | Presentation for this project |
| atm\_controller.v | Verilog Module for ATM Controller |
| tb\_atm\_controller.v | Verilog Testbench for ATM Controller module |